Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1-19 (Canceled)

20. (Currently Amended) A booster circuit connecting and boosting basic charge pump cells disposed respectively at N stages, the booster circuit comprising:

said basic charge pump cells each including at least a first MISFET, a second MISFET, a third MISFET, and a first capacitor, a fourth MISFET, and a second capacitor,

wherein a back gate of said first MISFET is connected to a first node, and a source-drain path thereof is connected between a second node and a third node,

a back gate of said second MISFET is connected to said first node, and a source-drain path thereof is connected between said first node and said second node,

a back gate of said third MISFET is connected to said first node, and a source-drain path thereof is connected between said first node and said third node,

one end of said first capacitor is connected to said third node, and a first clock with an amplitude of an operating voltage is inputted to the other end thereof,

said third node is connected to a second node of said basic charge pump cell

at a next stage,

one end of said second capacitor is connected to a gate of said first MISFET, and a second clock, having a voltage amplitude larger than that of a sum of said operating voltage and a threshold voltage of said first MISFET and being a reversed phase to said first clock, is inputted to the other end thereof, and

a back gate of said fourth MISFET is connected to said first node, a source-drain path thereof is connected between said second node and the gate of said first MISFET, and, for each of the N stages other than a first stage, a gate thereof is connected said one end of said second capacitor configuring said basic charge pump cell at a preceding stage.

21. (Currently Amended) A booster circuit connecting and boosting basic charge pump cells disposed respectively at N stages, the booster circuit comprising:

said basic charge pump cells each including at least a first MISFET, a second MISFET, a third MISFET, a first capacitor, a fourth MISFET, and a second capacitor,

wherein a back gate of said first MISFET is connected to a first node, and a source-drain path thereof is connected between a second node and a third node,

a back gate of said second MISFET is connected to said first node, and a source-drain path thereof is connected between said first node and said second node,

a back gate of said third MISFET is connected to said first node, and a source-drain path thereof is connected between said first node and said third node,

one end of said first capacitor is connected to said third node, and a first clock with an amplitude of an operating voltage is inputted to the other end thereof,

said third node is connected to a second node of said basic charge pump cell

at a next stage,

one end of said second capacitor is connected to a gate of said first MISFET, and a second clock, having a voltage amplitude larger than that of a sum of said operating voltage and a threshold voltage of said first MISFET and having a same phase as said first clock, is inputted to the other end thereof, and

a source-drain path of said fourth MISFET is connected between said third node and the gate of said first MISFET, and, for each of the N stages other than a first stage, a gate thereof is connected said one end of said second capacitor configuring said basic charge pump cell at a preceding stage.

22. (Previously Presented) The booster circuit according to claim 20, wherein said first, second, third, fourth MISFETs are n-type MISFETs, and a voltage is boosted on a positive side.

23. (Previously Presented) The booster circuit according to claim 20, wherein said first, second, third, and fourth MISFETs are p-type MISFETs, and a voltage is boosted on a negative side.

24. (Previously Presented) The booster circuit according to claim 21, wherein said first, second, third, and fourth MISFETs are n-type MISFETs, and a voltage is boosted on a negative side.

25. (Previously Presented) The booster circuit according to claim 21, wherein said first, second, third, and fourth MISFETs are p-type MISFETs, and a voltage is boosted on a positive side.

26. (Previously Presented) The booster circuit according to claim 20, further comprising:

a twice boosted clock generating circuit for generating a clock of a voltage twice as much as said operating voltage, and

wherein said twice boosted clock generating circuit generates said second clock.

27. (Previously Presented) The booster circuit according to claim 21,

wherein said first clock inputted to said basic charge pump cells at odd-numbered stages and said first clock inputted to said basic charge pump cells at even-numbered stages are opposite in phase, and

said second clock inputted to said basic charge pump cells at the odd-numbered stages and said second clock inputted to said basic charge pump cells at the even-numbered stages are opposite in phase.

28. (Previously Presented) A booster circuit connecting and boosting basic charge pump cells disposed respectively at N stages, the booster circuit comprising:

said basic charge pump cells each including:

an n-type transfer MISFET, and a first connection circuit for connecting a drain or source of said transfer MISFET, whichever is lower in potential, and a back gate of said transfer MISFET;

a circuit applying, to a gate of said transfer MISFET via a capacitance, a voltage having a voltage amplitude larger than that of a sum of an operating voltage and a threshold voltage of said transfer MISFET; and

a second connection circuit for connecting the gate of said transfer MISFET

and one of the drain and source thereof when said transfer MISFET is in an OFF state.

29. (Previously Presented) The booster circuit according to claim 28,

wherein said first connection circuit is configured by a first body controlled MISFET and a second body controlled MISFET, and

one of said first and second body controlled MISFETs is conducted, and the drain or source of said transfer MISFET, whichever is lower in potential, and the back gate of said transfer MISFET are connected.

30. (Previously Presented) A booster circuit connecting and boosting basic charge pump cells disposed respectively at N stages, the booster circuit comprising:

said basic charge pump cells each including:

a p-type transfer MISFET;

a first connection circuit for connecting a drain or source of said transfer MISFET, whichever is lower in potential, and a back gate of said transfer MISFET;

a circuit applying, to a gate of said transfer MISFET via a capacitance, a voltage having a voltage amplitude larger than that of a sum of an operating voltage and a threshold voltage of said transfer MISFET; and

a second connection circuit for connecting the gate of said transfer MISFET to one of the drain and source thereof when said transfer MISFET is in an OFF state.

31. (Previously Presented) The booster circuit according to claim 30,

wherein said first connection circuit is configured by a first body controlled MISFET and a second body controlled MISFET, and

one of said first and second body controlled MISFETs is conducted, and the drain or source of said transfer MISFET, whichever is lower in potential, and the back gate of said transfer MISFET are connected.

32. (Currently Amended) The booster circuit according to claim 20, further comprising:

a selection circuit for choosing which of plus or minus voltages is boosted.

33. (Previously Presented) The booster circuit according to claim 32,

Wherein said selection circuit is a circuit for connecting a second node of one of said basic charge pump cell at a first stage and said basic charge pump cell at a last stage to said operating voltage, and for connecting a third node of the other thereof to a ground potential.

34. (Previously Presented) The booster circuit according to claim 20, further comprising:

a serial-type charge pump,

wherein said serial-type charge pump outputs a second voltage from a first voltage outputted from said booster circuit.

35. (Previously Presented) A non-volatile memory executing at least one of reading, writing, and deletion in accordance with a voltage generated by the booster circuit according to claim 20.

36. (Previously Presented) An IC card having the non-volatile memory according to claim 35.

37. (Currently Amended) The booster circuit according to claim 28,

wherein said second connection circuit is a gate voltage set MISFET, whose drain-source path is connected between the gate and the drain or source of said transfer MISFET, and, for each of the N stages other than a first stage, in which a gate voltage of said transfer ~~MOS~~ MISFET in the pump cell at a preceding stage is applied to a gate value thereof.

38. (Currently Amended) The booster circuit according to claim 30,

wherein said second connection circuit is a gate voltage set MISFET, whose drain-source path is connected between the gate and the drain or source of said transfer MISFET, and, for each of the N stages other than a first stage, in which a gate voltage of said transfer ~~MOS~~ MISFET in the pump cell at a preceding stage is applied to a gate value thereof.